Hale COLLAGE (NJIT Phys-780)
Topics in Solar Observation Techniques

Lecture 03: Astronomical Detectors

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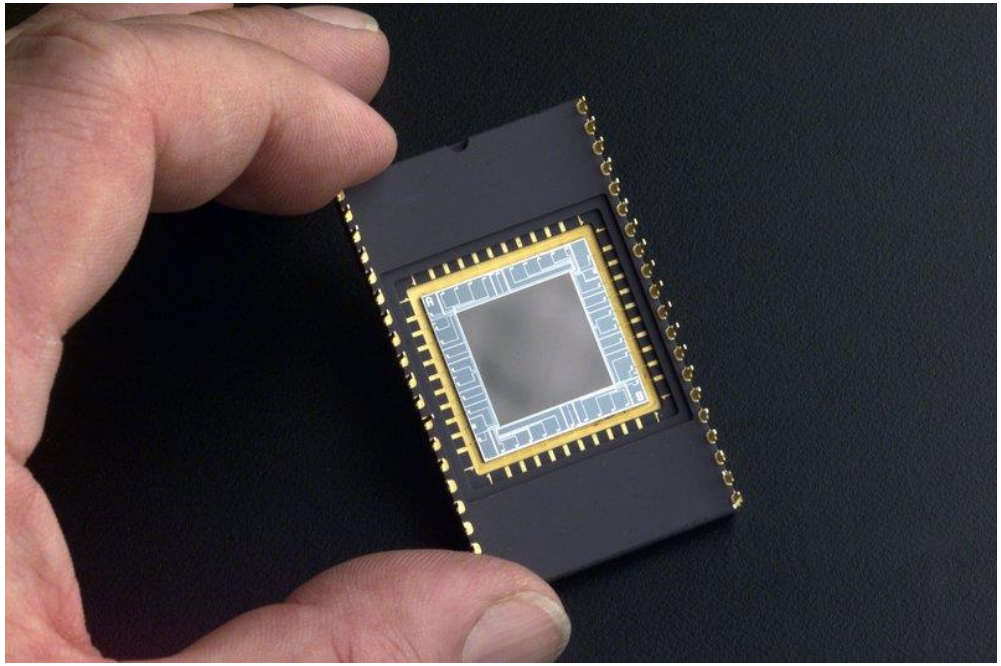


Why not Eyes or Films

Solid State Devices

- *no loss of sensitivity to light during exposure*
- *no minimal light intensity required to detect a target*
- *high efficiency of light detection (up to 50 ~ 90%, though device- and wavelength-dependent)*
- *signal is proportional to light intensity*
- *large dynamic range (typically 16-bit)*
- *picture elements (pixels) are regularly spaced*
- *ready for digital processing*

Solid State Device

- *A Solid State Device is a photosensitive device that converts light signals into digital signals*
  - *An incoming photon kicks an electron in the conduction band*
  - *The read-out system gives a digital signal*
- *Typically, the three main types in astronomical imaging are*
  - *CCD: Charge-Coupled Device*
  - *CMOS: Complementary Metal-Oxide Semiconductor*
  - *IRFPA: Infrared Focal Plane Array*
- *Basic Operating Principle*
- *Performance of Solid State Detectors*
- *Observation with Solid State Detectors*

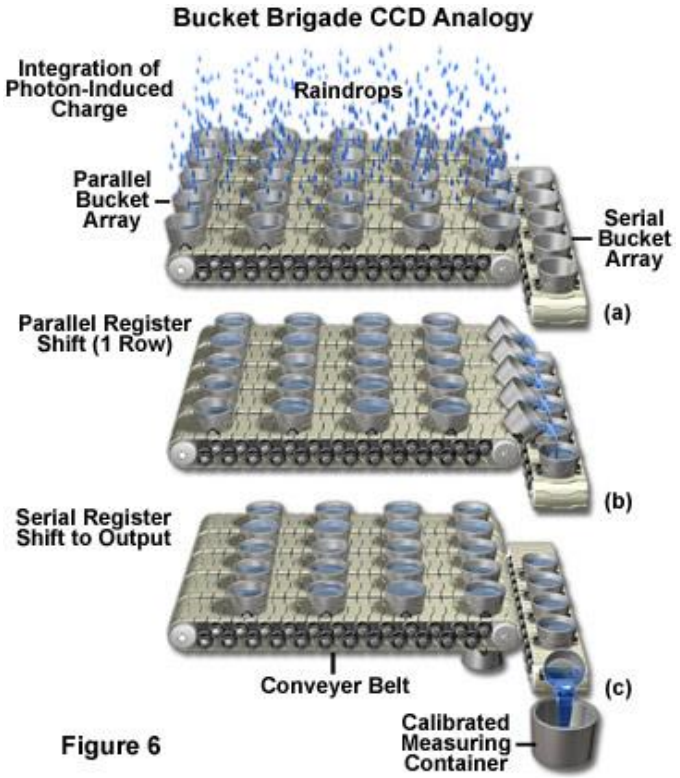
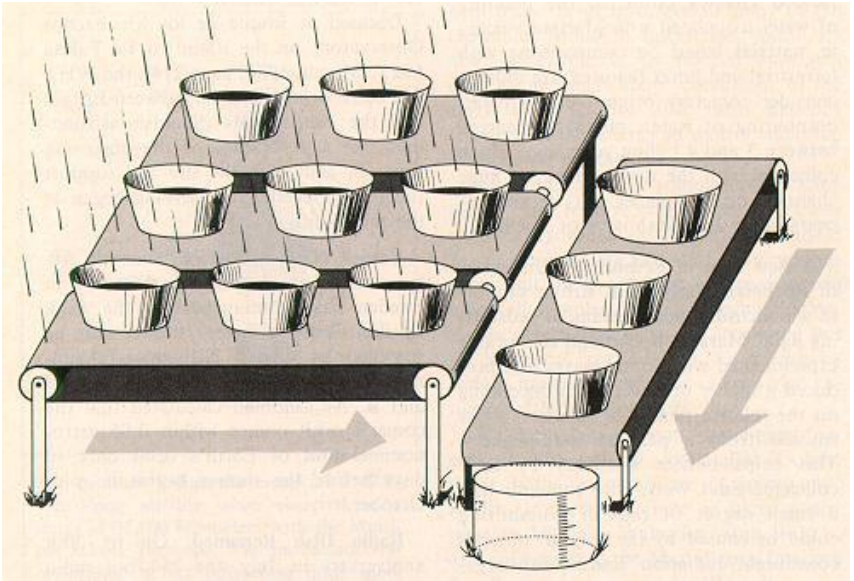


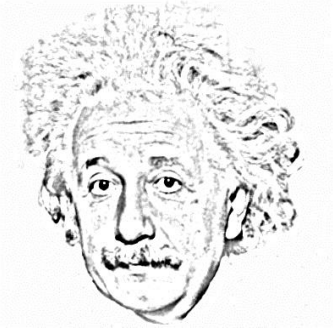
Figure 6

1. Basic Operating Principle

- *Step 0 - Light into Detector*
- *Step 1 - Charge Generation*
- *Step 2 - Charge Collection*
- *Step 3 - Charges Transfer*
- *Step 4 - Charge-to-Voltage Conversion*
- *Step 5 - Digitization*

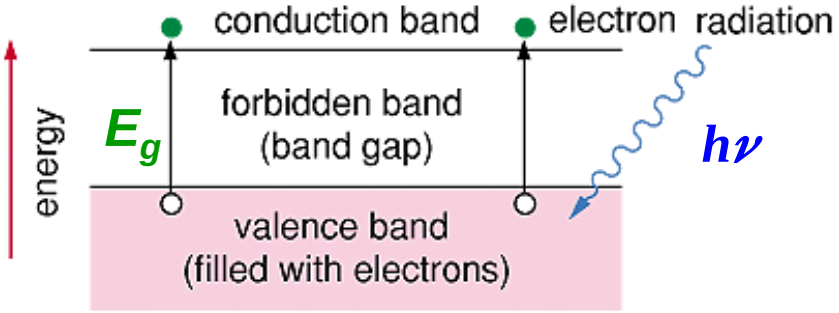


1.1 Charge Generation



- *For an electron to be excited from valence band to conduction band*

$$h\nu \geq E_g$$



  - ***h*** *= 6.63 ×10^{-34} Joule ·s (Planck constant)*
  - ***ν = c / λ*** *(Frequency of light)*
  - *E_g: electron-volts (Energy gap of material)*

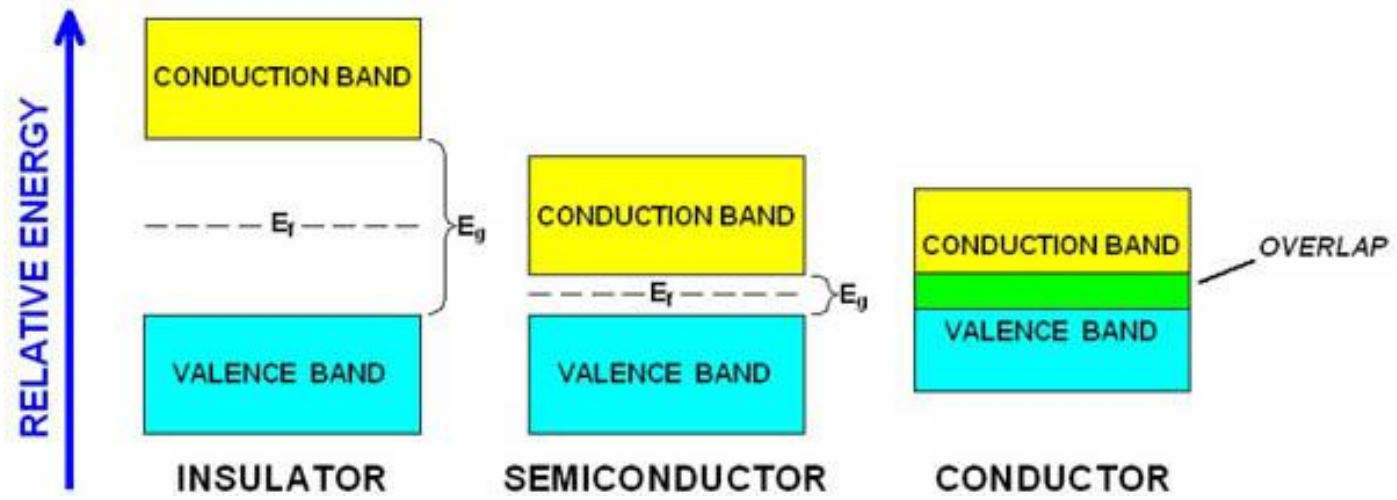
- *Long wavelength cut-off*

$$\lambda \leq \frac{1.238}{E_g\,(eV)} = \lambda_{cut-off}\,(\mu m)$$

- *Silicon: E_g = 1.12 eV, $\lambda_{cut\text{-}off}$ = ?*

Band Gap Energy

- *Minimum energy to elevate an electron into conduction is the "band gap energy".*
- *semiconductors have a narrow gap between the valence and conduction bands.*



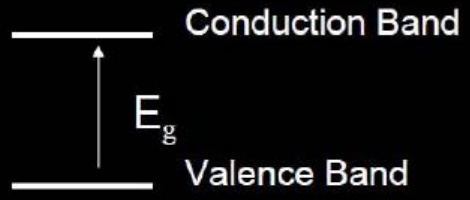
- *Semiconductors allow for photo-sensitive circuits (photon absorption adds energy to electron).*

Detector Family

For an electron to be excited from the valence band to the conduction band

$h\nu > E_g$

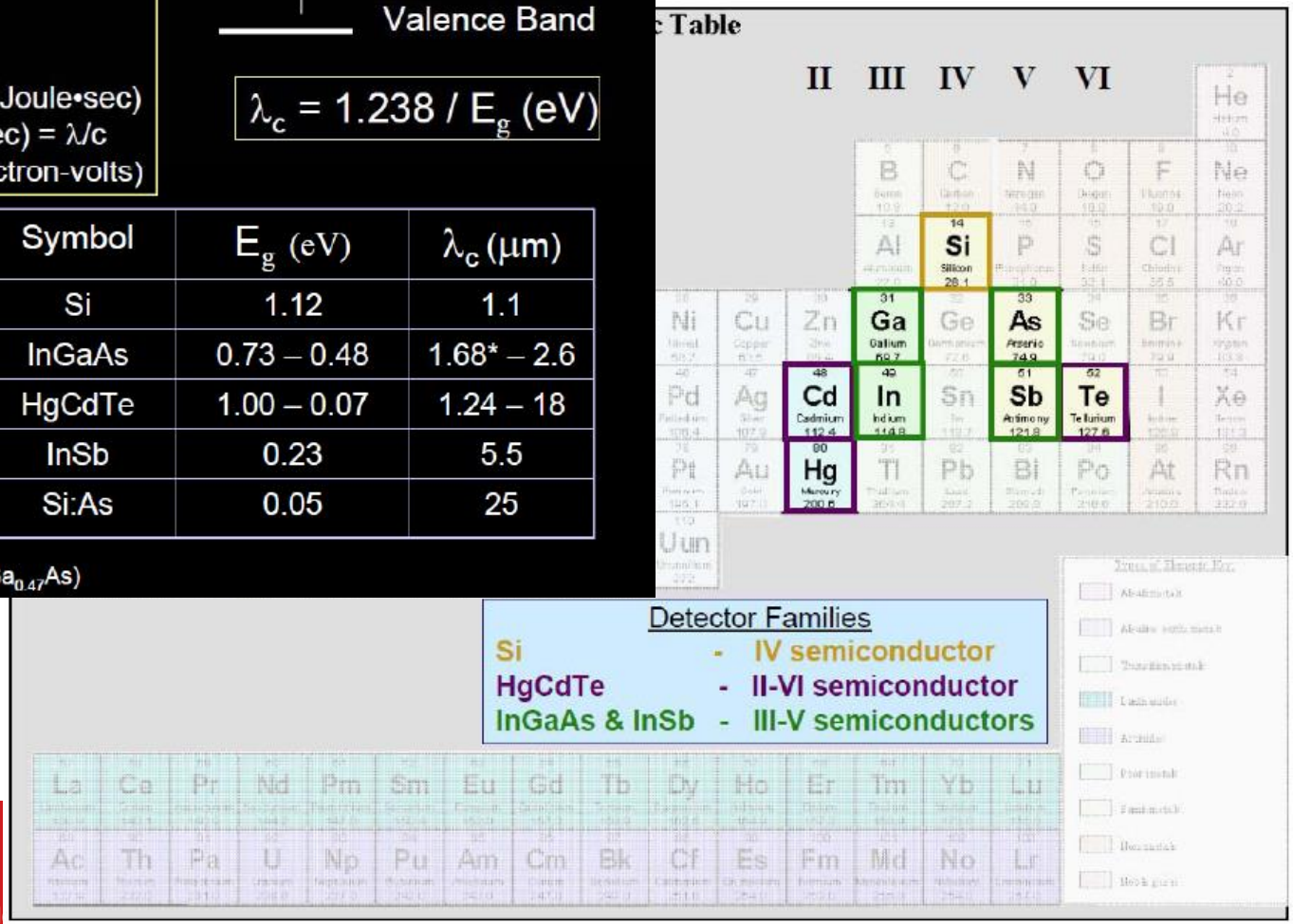
h = Planck constant (6.6310-^{34} Joule•sec)
ν = frequency of light (cycles/sec) = λ/c
E_g = energy gap of material (electron-volts)



$\lambda_c = 1.238 / E_g$ (eV)

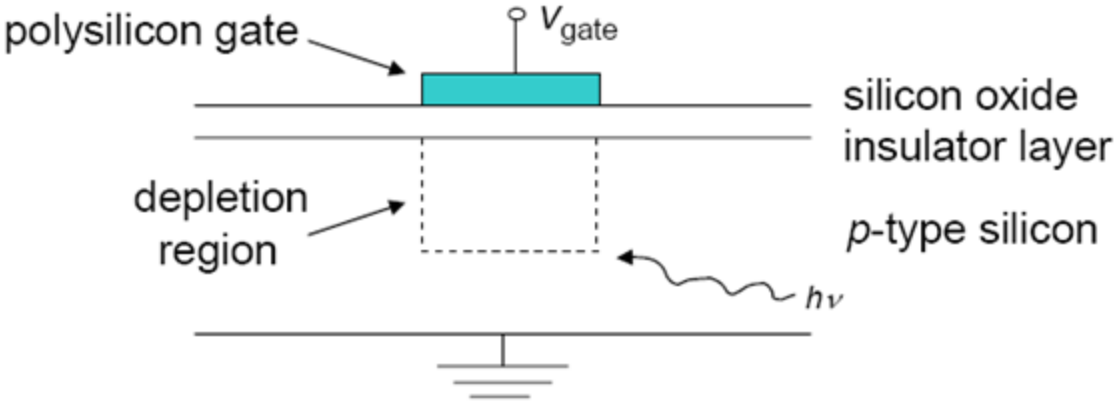
Material Name	Symbol	E_g (eV)	λ_c (μm)
Silicon	Si	1.12	1.1
Indium-Gallium-Arsenide	InGaAs	0.73 – 0.48	1.68* – 2.6
Mer-Cad-Tel	HgCdTe	1.00 – 0.07	1.24 – 18
Indium Antimonide	InSb	0.23	5.5
Arsenic doped Silicon	Si:As	0.05	25

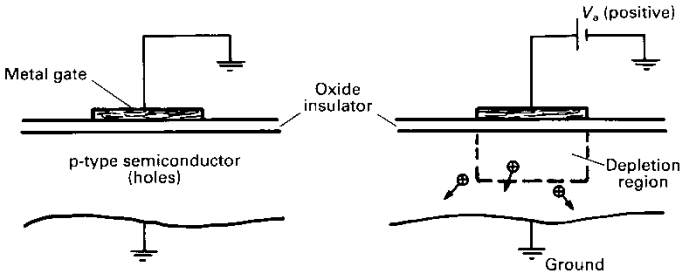
*Lattice matched InGaAs ($In_{0.53}Ga_{0.47}As$)



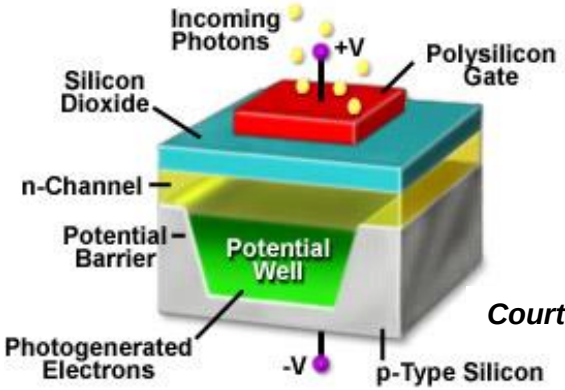
1.2 Charge Collection

- *A Metal-Oxide-Semiconductor (MOS) capacitor has a potential difference between two metal plates separated by an insulator.*





Metal Oxide Semiconductor (MOS) Capacitor



Courtesy: RIT Courses

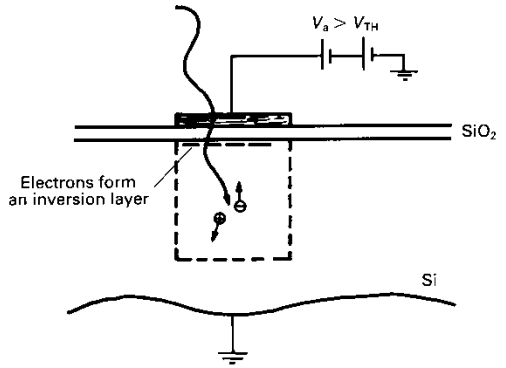


Fig. 6.7. A single metal-oxide-semiconductor (MOS) storage well, the basic element in a CCD.

MOS and Potential Well

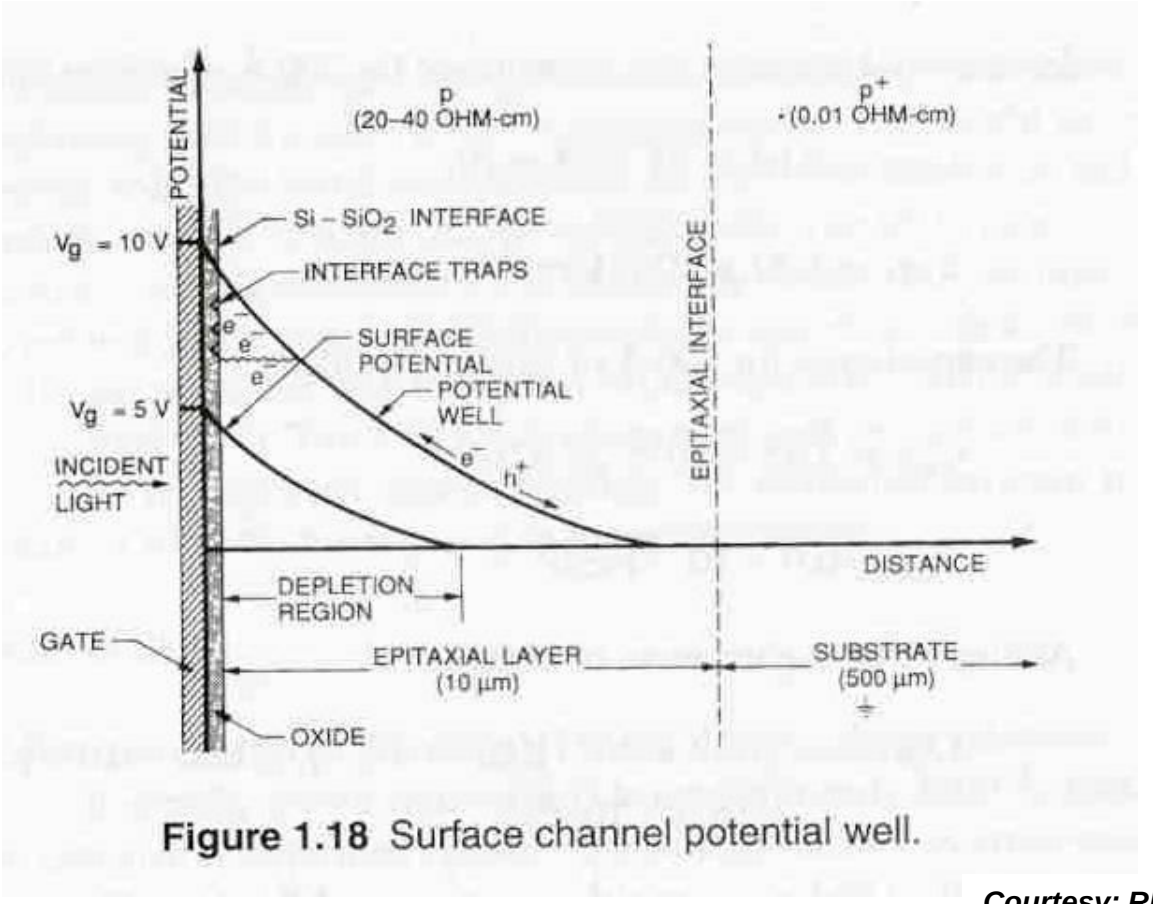


Figure 1.18 Surface channel potential well.

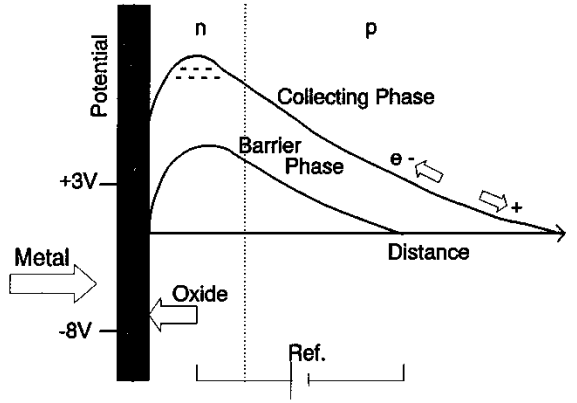
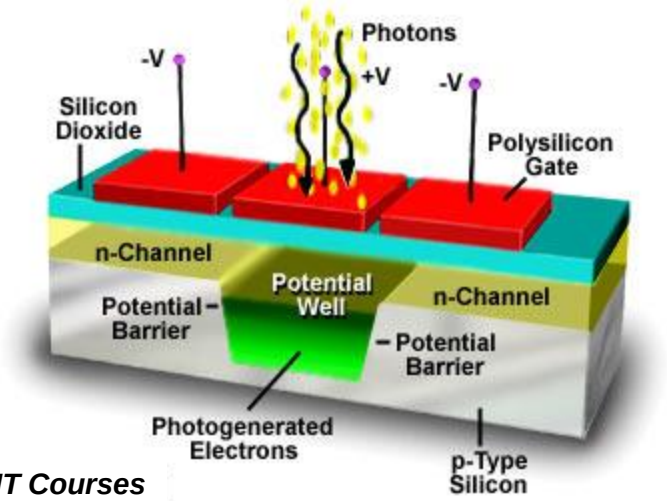


Fig. 6.12. (b) The collection layer lies well below the surface at the overlap between the gate depletion and the depletion of the pn junction. Courtesy Jim Janesick.

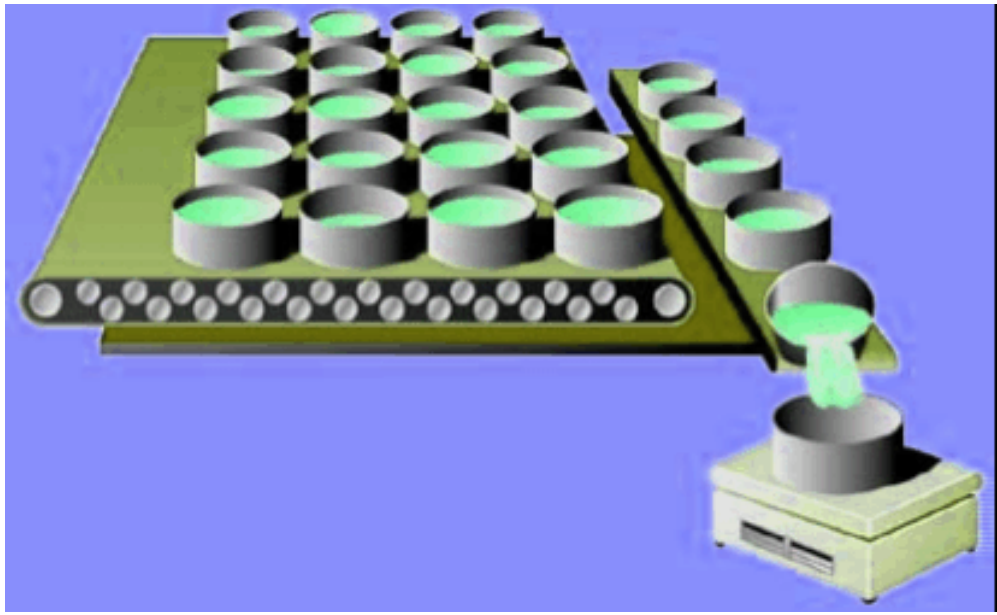
Metal Oxide Semiconductor (MOS) Capacitor

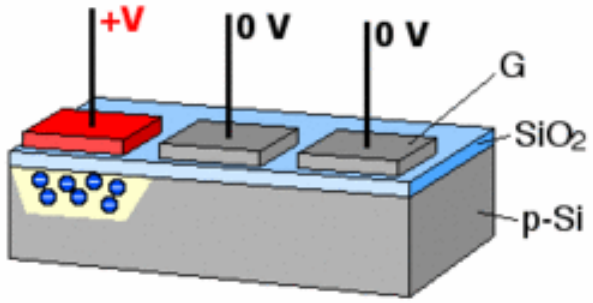


Courtesy: RIT Courses

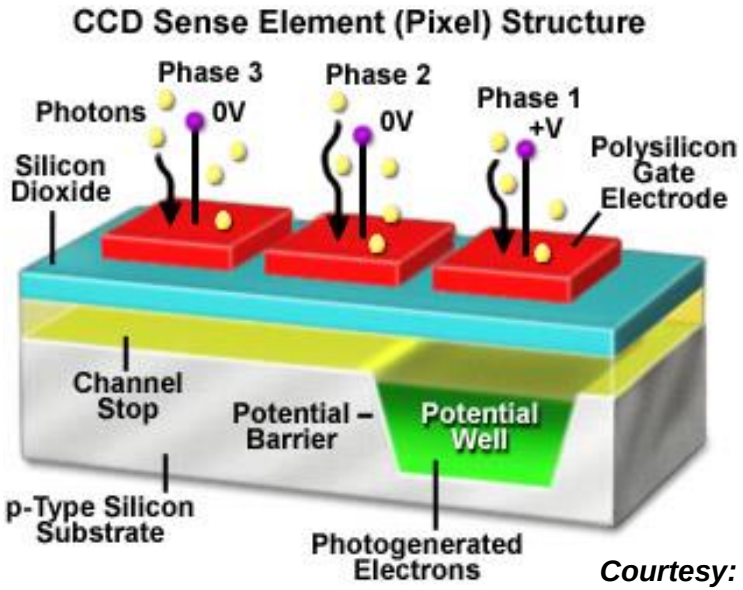
1.3 Charge Transfer

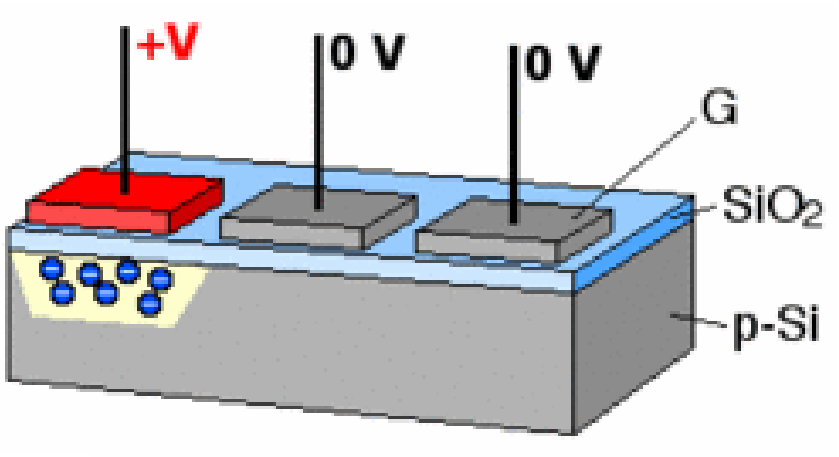
- *CCD Readout Architecture*
- *Pixel and Register*
- *CCD Phase Clocking*
- *Parallel Register*
- *Serial Register*





CCD Pixel and Register

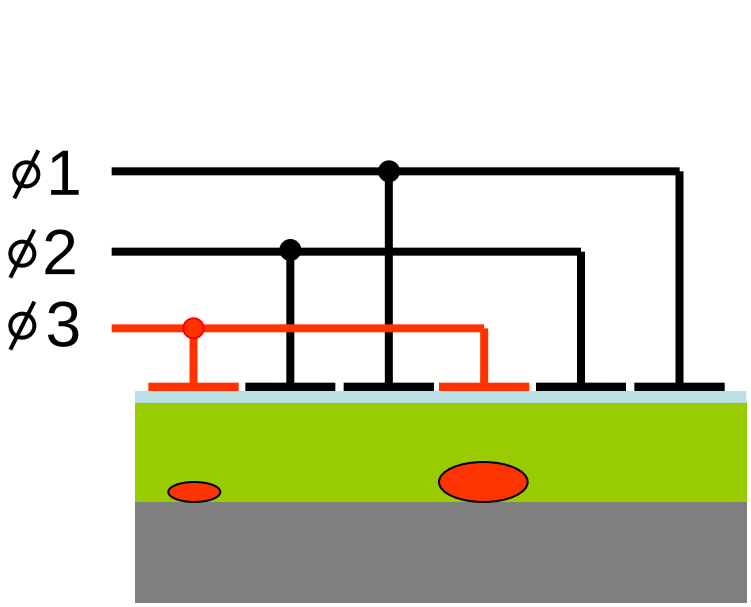


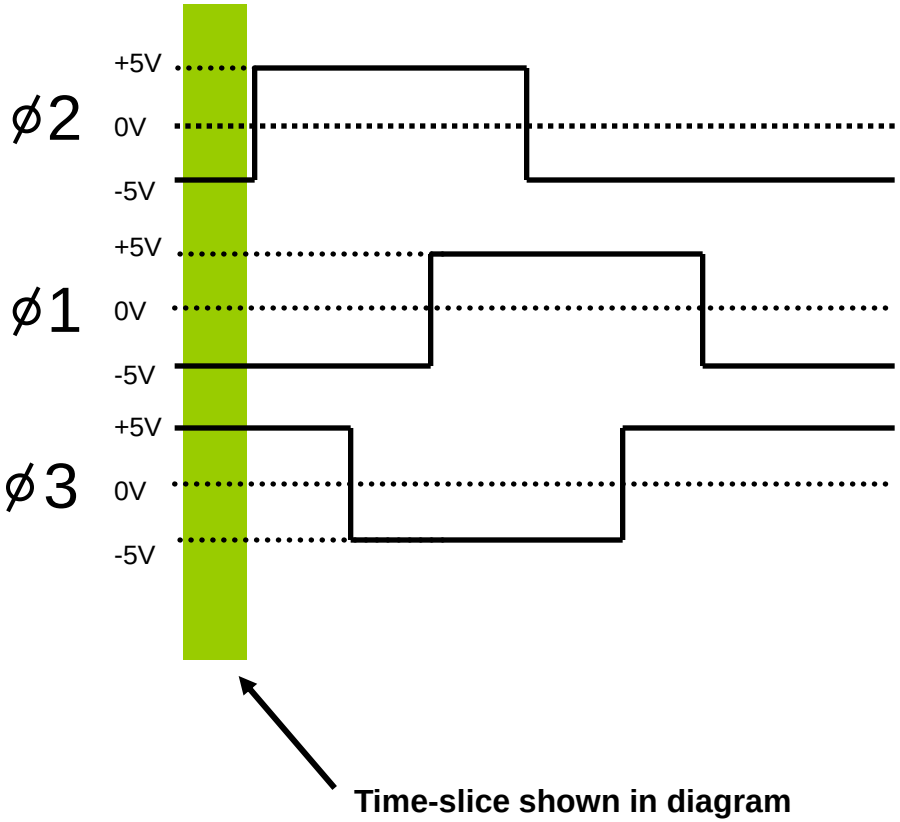


Courtesy: RIT Courses

- *MOS capacitors are the basic building blocks of the CCD*
- *Each pixel consists of several MOS capacitors*
- *MOS capacitors follow phase clock to transfer charges*

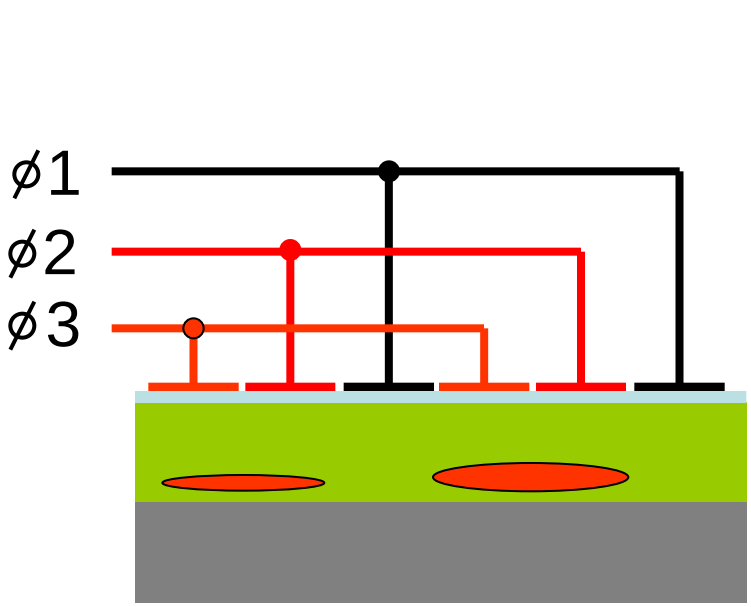
CCD Phased Clocking: Step 1

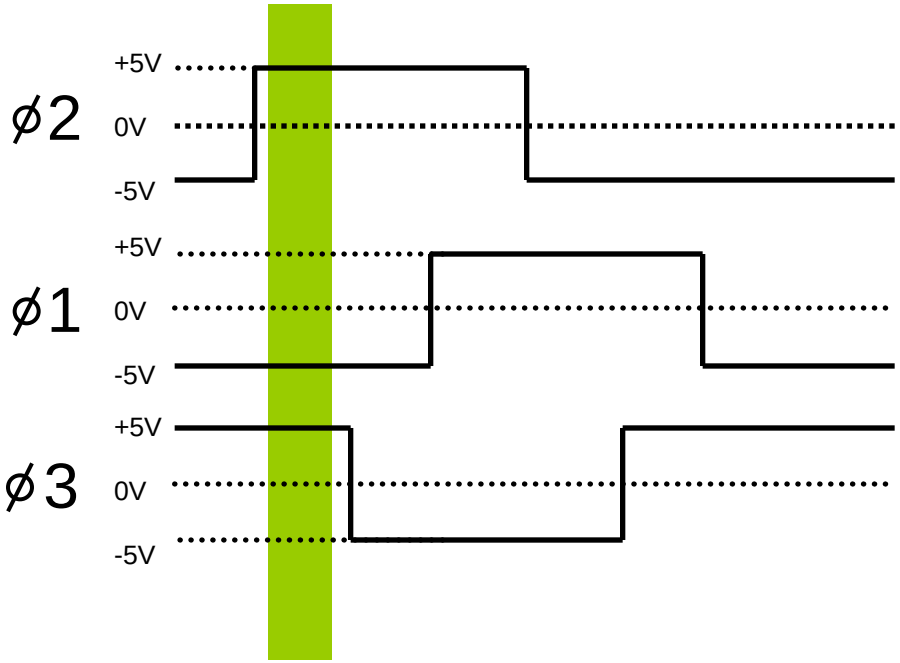




Courtesy: RIT Courses

CCD Phased Clocking: Step 2





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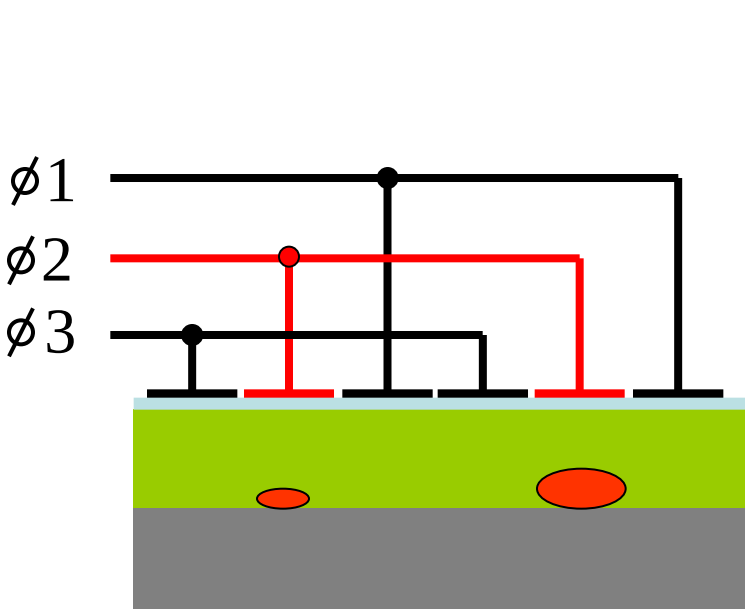
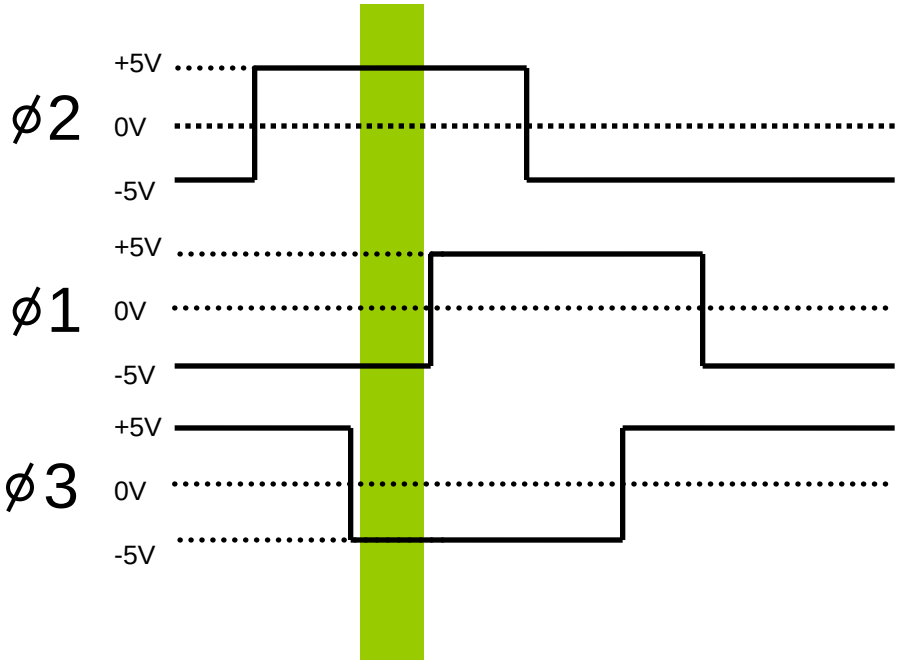
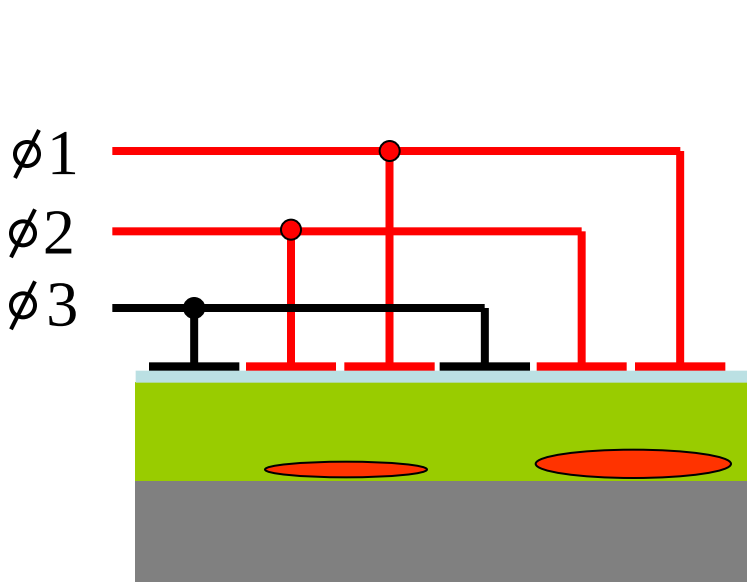
CCD Phased Clocking: Step 3

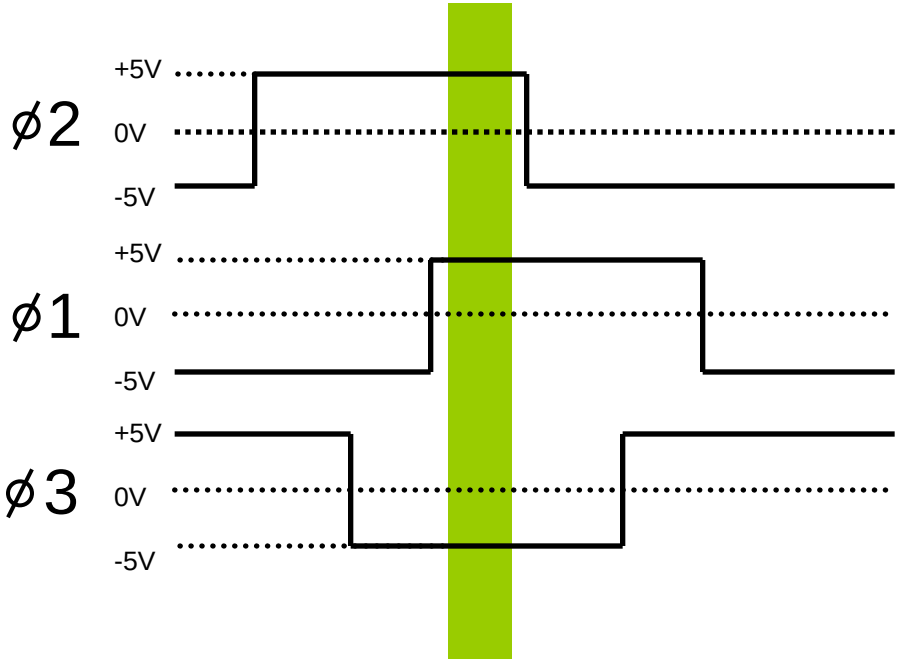




Courtesy: RIT Courses

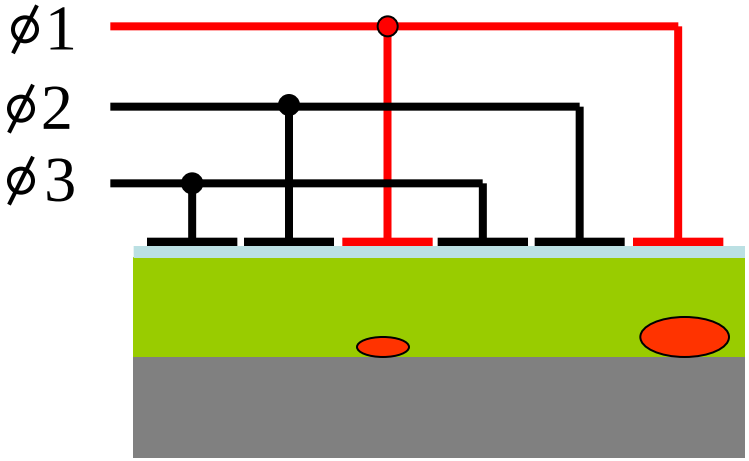
CCD Phased Clocking: Step 4

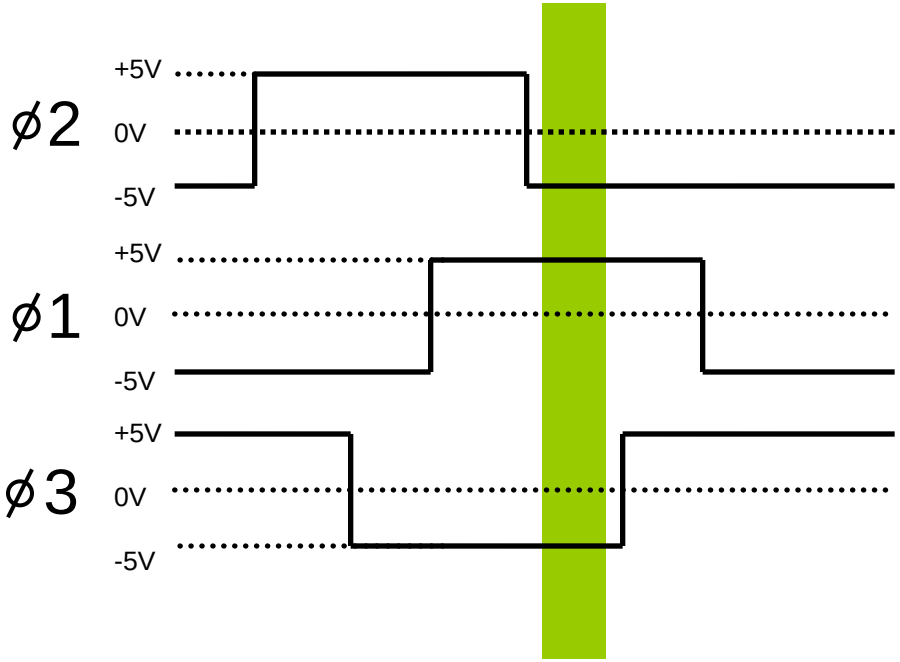




Courtesy: RIT Courses

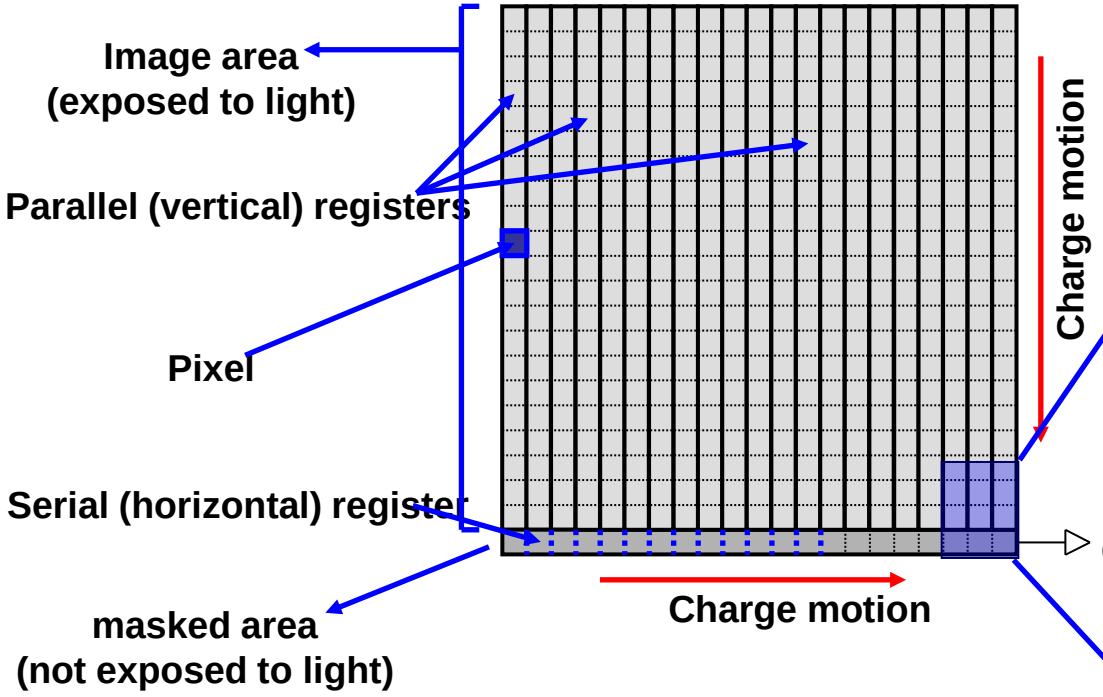
CCD Phased Clocking: Step 5

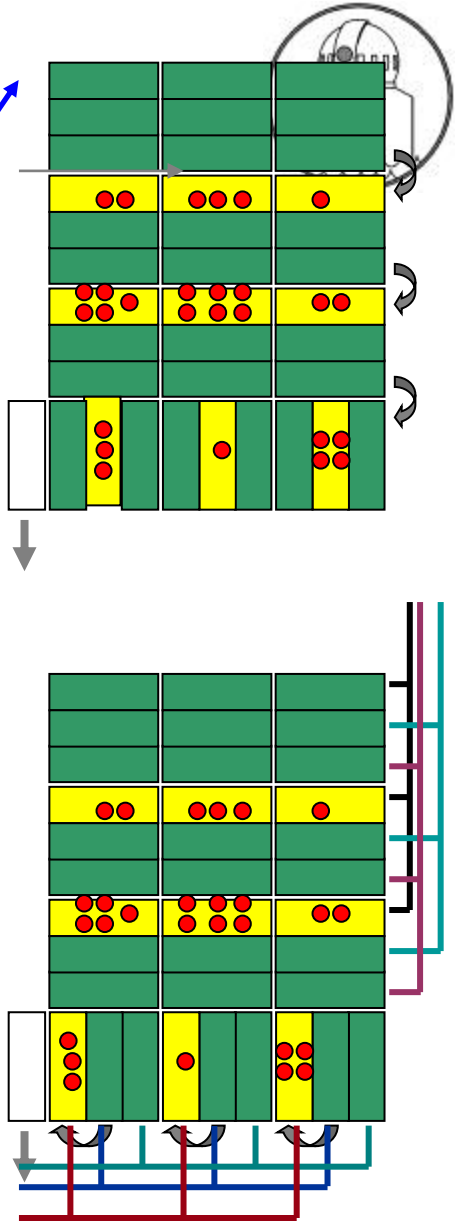




Courtesy: RIT Courses

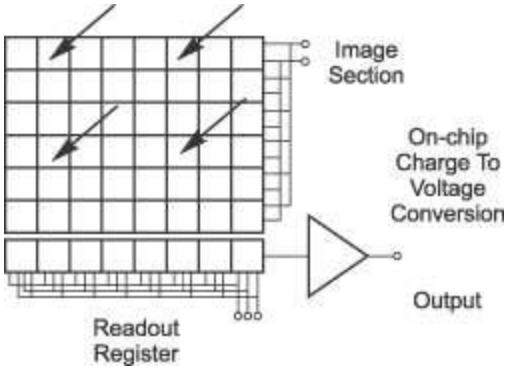
Parallel and Serial Registers

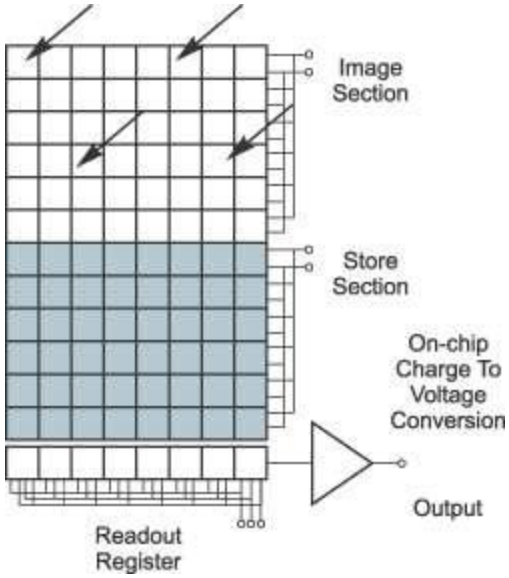


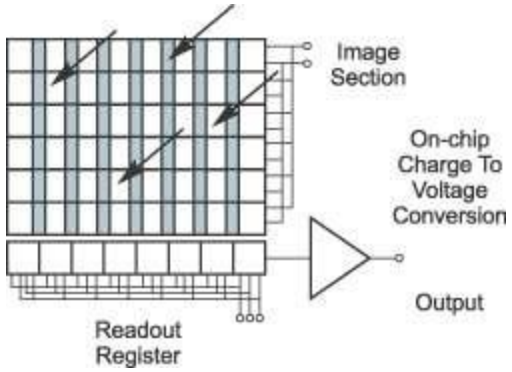


- *Parallel registers transfer charges vertically*
- *Serial registers transfer charges horizontally*
- *They operate at different frequencies*
- *For 3 by 3 CCD, $f_{vertical}$ = 10 Hz, f_{serial} = ?*

Other Types of Architecture

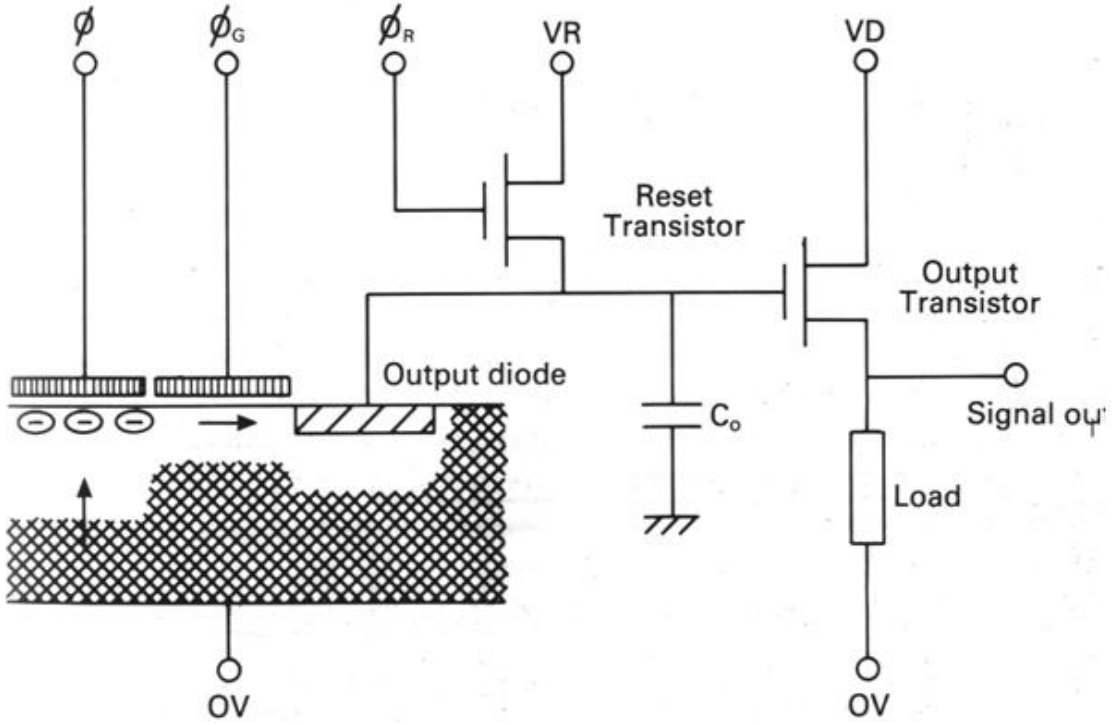






- *Full frame and frame transfer devices tend to be used for scientific applications.*
- *Interline transfer devices are used in consumer camcorders and TV systems.*
- *Frame transfer imager consists of two almost identical arrays, one devoted to image pixels and one for storage.*
- *Interline transfer array consists of photodiodes separated by vertical transfer registers that are covered by an opaque metal shield.*

1.4 Charge-to-Voltage Conversion



- *Each pixel's collected charge is sensed and amplified by an output amplifier*
- *They are designed to have low noise and built into the silicon circuitry*
- *Typical values are in the range of 0.5 to 4 microvolts per electron*

1.5 Digitization (A/D Conversion)

- *Output voltage from a given pixel is converted to a digital number (ADUs – analog-to-digital units)*
- *A/D (ADC, analog-to-digital converter) performs the conversion of output voltage signal to a digital number*
- *Digitization circuits are complicated and not included in a CCD chip, "off-chip" circuit.*
- *Digital output values can only be integer numbers with digital bits:*
  - *8 bits: $2^8 = 256$*
  - *10 bits: $2^{10} = 1024$*
  - *14 bits: $2^{14} = 16383$*
  - *16 bits: $2^{16} = 65535$*

- *Ultimate readout speed depends on how fast the process of pixel examination and A/D conversion can take place*
  - *At a readout rate of 50 μs/pixel (~ 20 kHz), how long does it take over to read out a 2048 by 2048 CCD ?*

2. Performance of CCD

- ***Charge Generation***
  - *QE – Quantum Efficiency*
  - *Dark Current*
- ***Charge Collection***
  - *Pixel Size*
  - *On-Chip Pixel Binning*
  - *Full Well Capacity*
- ***Charge Transfer***
  - *CTE – Charge Transfer Efficiency*
  - *Defects*
- ***Charge Detection***
  - *Readout Noise*
  - *Linearity*
  - *Gain and Dynamic Range*

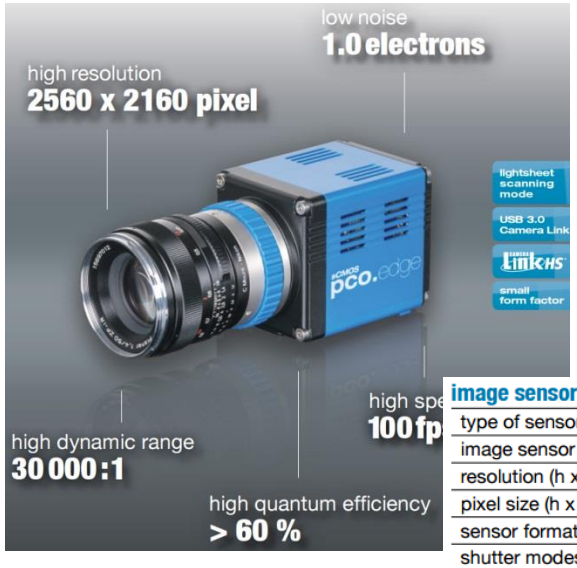
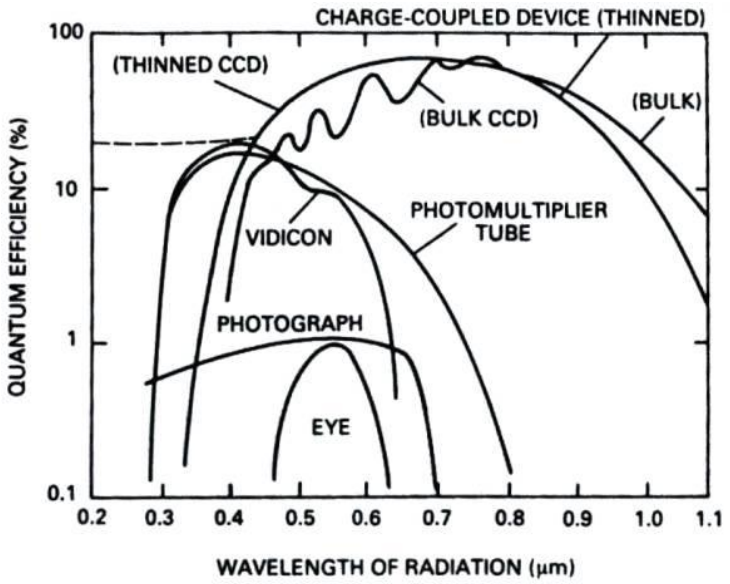


image sensor	
type of sensor	scientific CMOS (sCMOS)
image sensor	CIS2521
resolution (h x v)	2560 x 2160 pixel
pixel size (h x v)	6.5 µm x 6.5 µm
sensor format / diagonal	16.6 mm x 14.0 mm / 21.8 mm
shutter modes	rolling shutter (RS) with free selectable readout modes, global/snapshot shutter (GS), global reset - rolling readout (GR)
MTF	76.9 lp/mm (theoretical)
fullwell capacity (typ.)	30 000 e⁻
readout noise[1]	1.0_{med} /1.4_{rms} e- RS 3.1_{med} /3.2_{rms} e- GS 1.0_{med} /1.4_{rms} e- GR
dynamic range (typ.)	30 000 : 1 (89.5 dB)
quantum efficiency	> 60 % @ peak
spectral range	370 nm .. 1100 nm
dark current (typ.)	< 0.5 e⁻/pixel/s RS/GR @ 5 °C < 0.8 e⁻/pixel/s GS @ 5 °C
DSNU	< 0.3 e⁻ rms
PRNU	< 0.2 %
anti blooming factor	> 10000

2.1 Quantum Efficiency

- *QE: the percentage of photons hitting the photoreactive surface that will produce an electron-hole pair .*
- *QE is an accurate measurement of device's electrical sensitivity to light.*
- *QE is a function of wavelength.*
- *QE is often measured over a range of different wavelengths*
- *Film typically has a QE of less than 10%.*
- *CCDs have a QE of well over 90% at some wavelength.*
- *QE depends on many factors, such as the gate structure, surface reflection, illuminating way …*

$$QE = \frac{electrons\ /\ \sec}{photons\ /\ \sec}$$



Front or Back Side Illumination

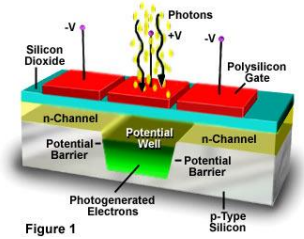
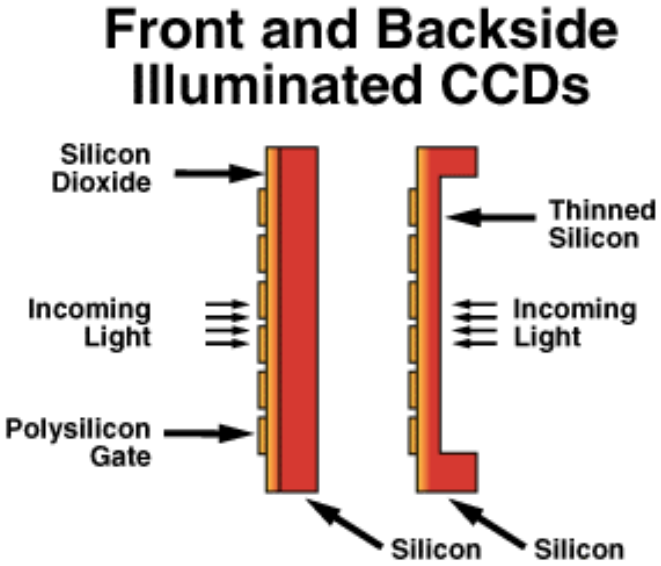


Figure 1

- *Front side illumination: CCDs are illuminated through the electrodes. Electrodes are semi-transparent, but some losses occur.*
- *Back side illumination: CCDs are illuminated from the back side.*
- *Front-side illuminated device: relatively low QE, filling factor < 1.*
- *Back-side illuminated device (or thinned devices): high QE* and *physically thinned to about 15 microns, filling factor close to 1.*



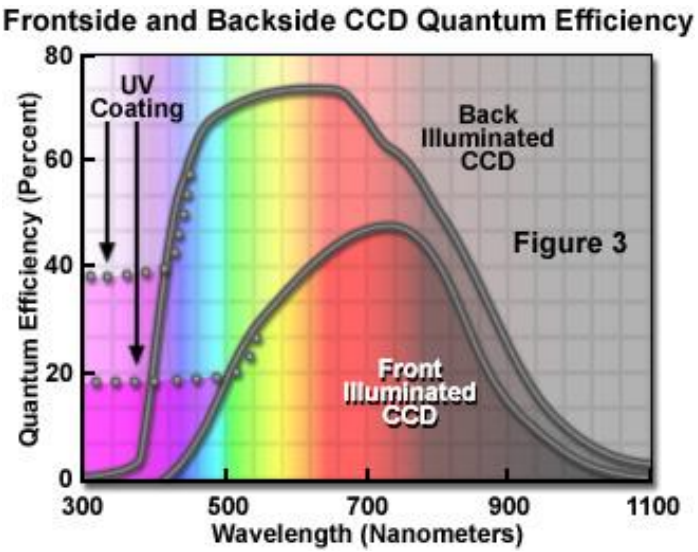
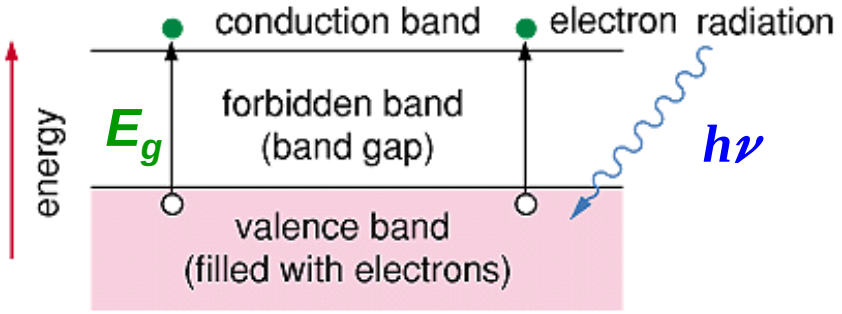
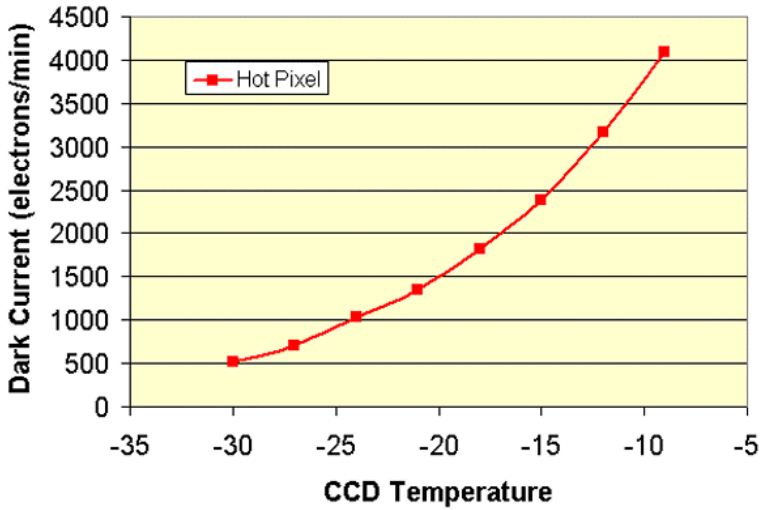


Figure 3

2.2 Dark Current

- *When thermal agitation is high enough, electrons get free from the valence band.*
- *They become collected within the potential well of a pixel.*
- *These dark current electrons become part of the signal, indistinguishable from object photons.*
- *Dark current is a strong function of the temperature of the device.*
- *At room temperature, dark current of a typical CCD is 25,000 e-/pixel/sec.*
- *Darks are more serious in IRFPAs than that in Si CCD/CMOS camera*



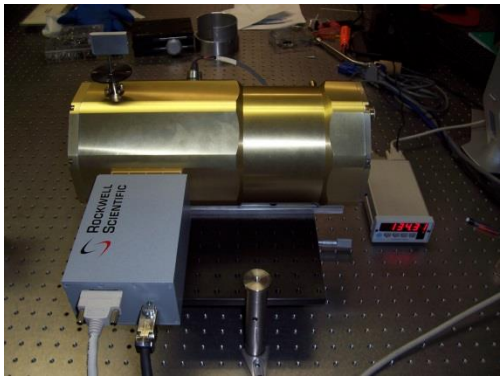


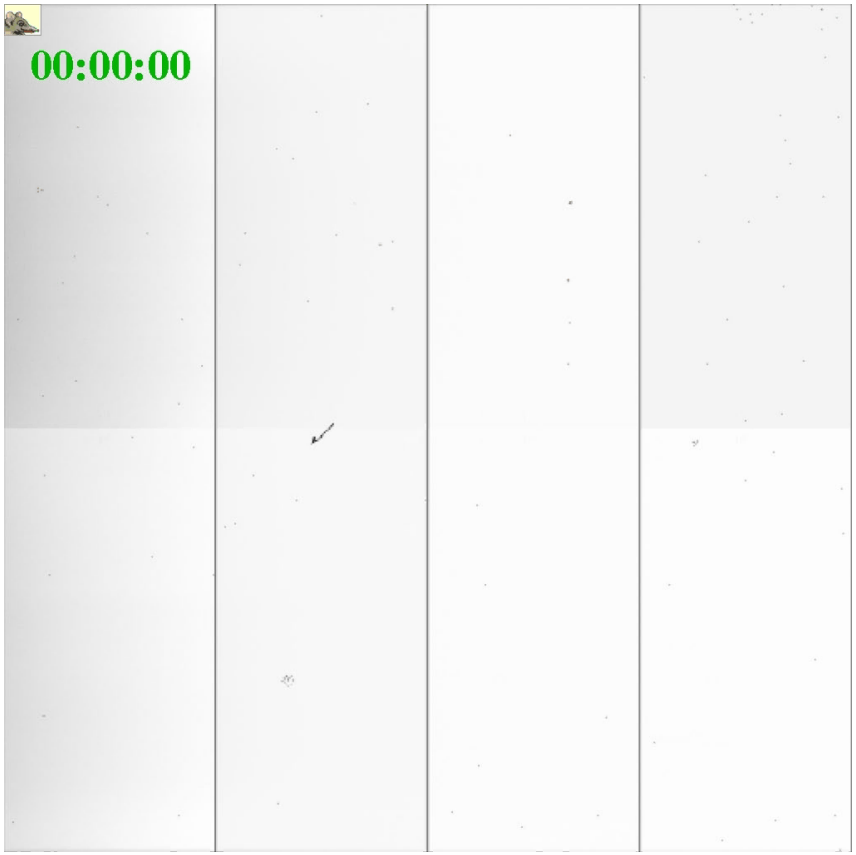
Minimize Dark Current

- *Dark noise has a Poisson distribution*

$$N_D = \sqrt{dark\ current}$$

- *LN2 (Liquid Nitrogen) cooling*
  - *Dewar in vacuum and LN2 in dewar*
  - *Cool CCD chip to -100℃*
  - *Cool IRFPA to 77 Kelvin*
- *Thermoelectric cooling*
  - *Cool CCD to -20 to -50 ℃*





2.3 Full Well Capacity

- *Well capacity is defined as the maximum charge that can be held in a pixel*
- *The physically larger the pixel (both in area and in thickness) the more charge that it can collect and store.*
- *"Saturation" is the term that describes when a pixel has accumulated the maximum amount of charge that it can hold*
- *Full well capacity in a CCD is typically ~100,000 e-/pixel*
- *A rough rule of thumb is that well capacity is about 10,000 e-/μm^2.*
- *What will happen when the full well capacity of a pixel is exceeded?*

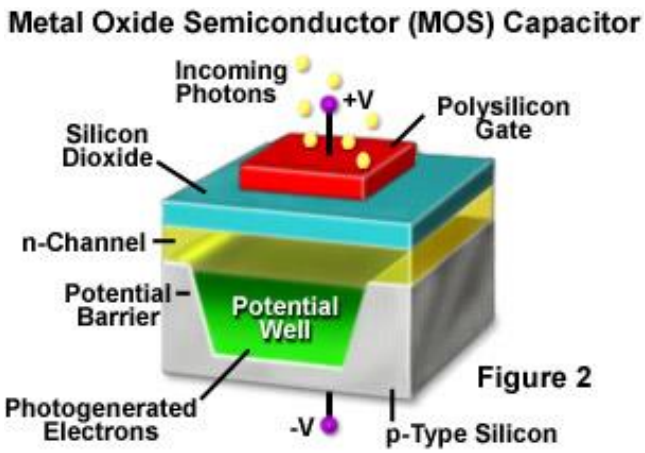
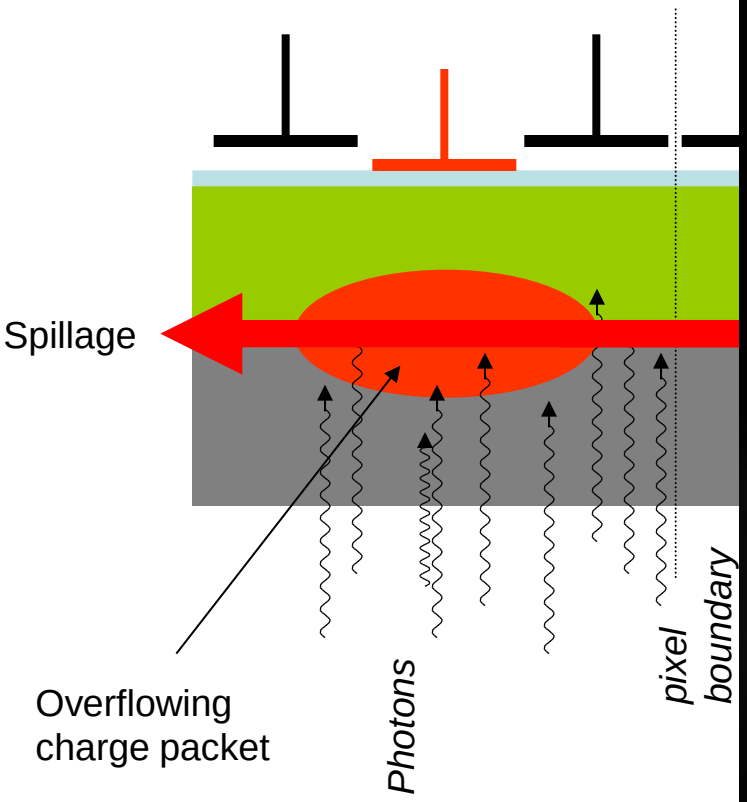
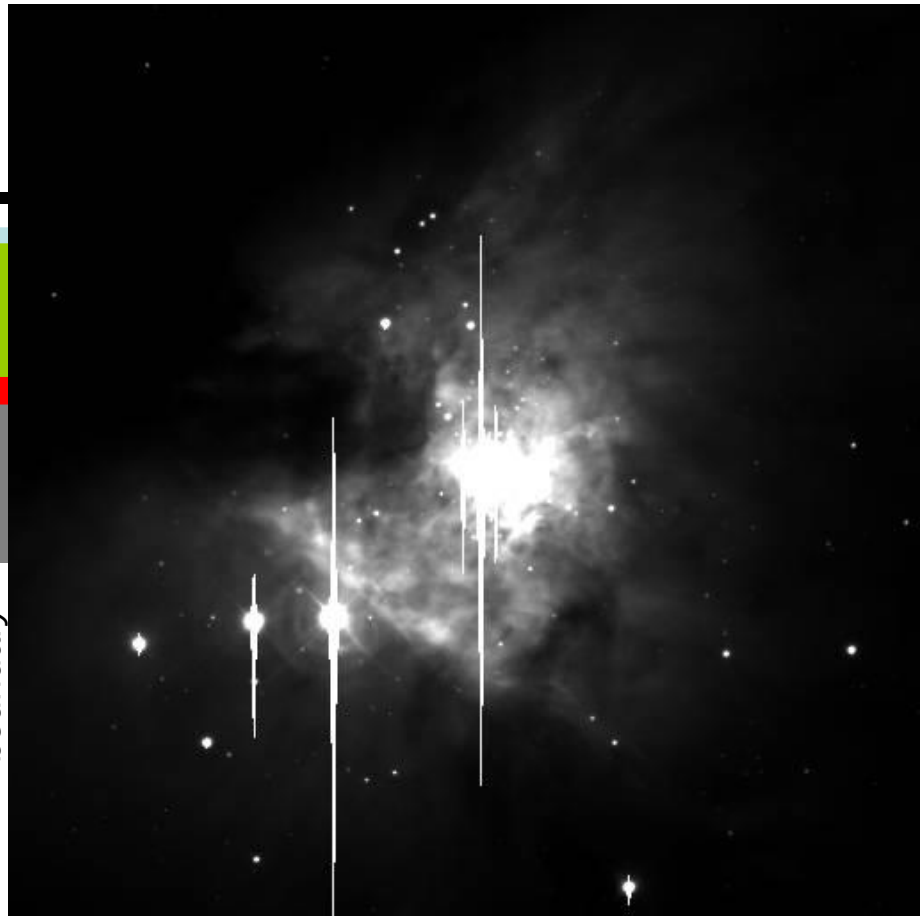


Figure 2

Blooming

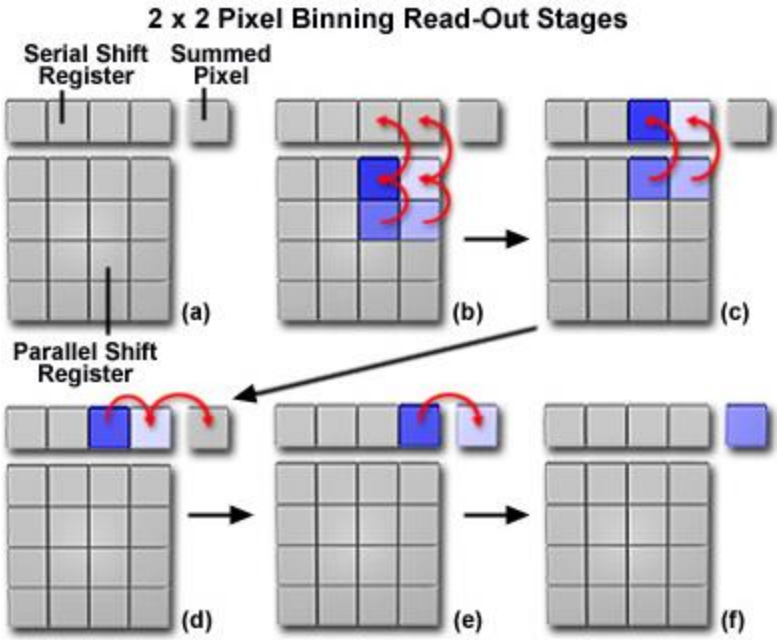
- *Bright objects can lead to the collection of too many charges in one pixel, causing pixel to overflow …*





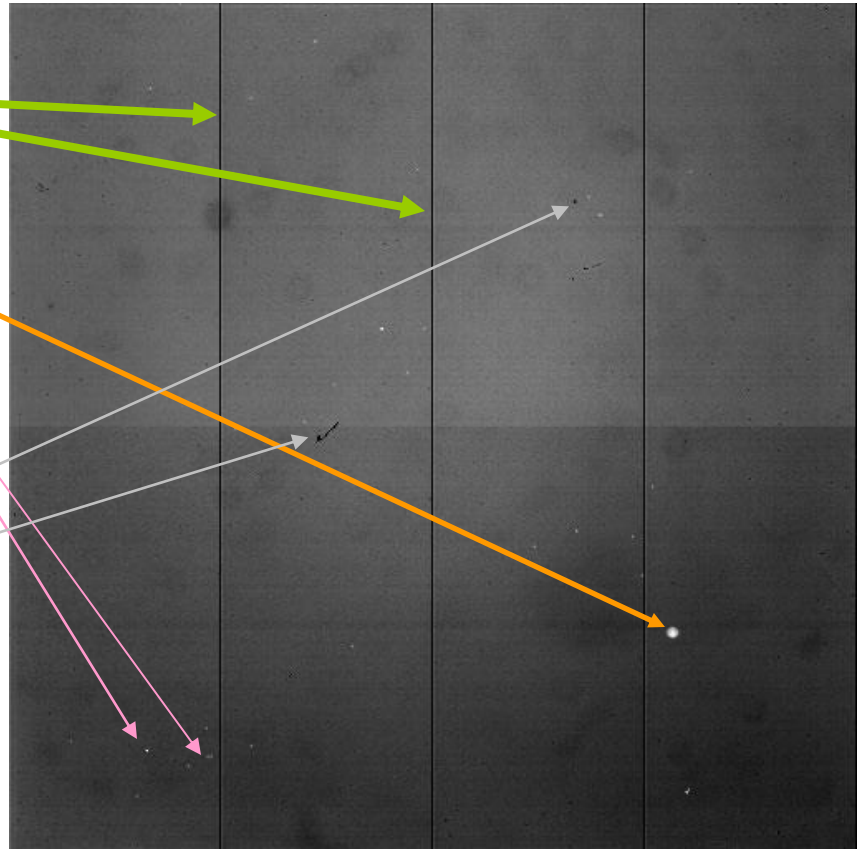
2.4 Pixel Binning

- *Pixel binning is a clocking scheme used to combine the charge collected by several adjacent CCD pixels .*
- *Binning process is performed on-chip, which assumes that accumulated charge is brought together and summed prior to amplification of analog signal and A/D conversion.*
- *Pixel binning reduces noise and image size, improves the signal-to-noise ratio and frame rate.*
- *Pixel can be binned in both directions.*
- *Serial register pixels can hold 5-10 times the charge of a single pixel.*
- *Pixel binning decrease image resolution.*



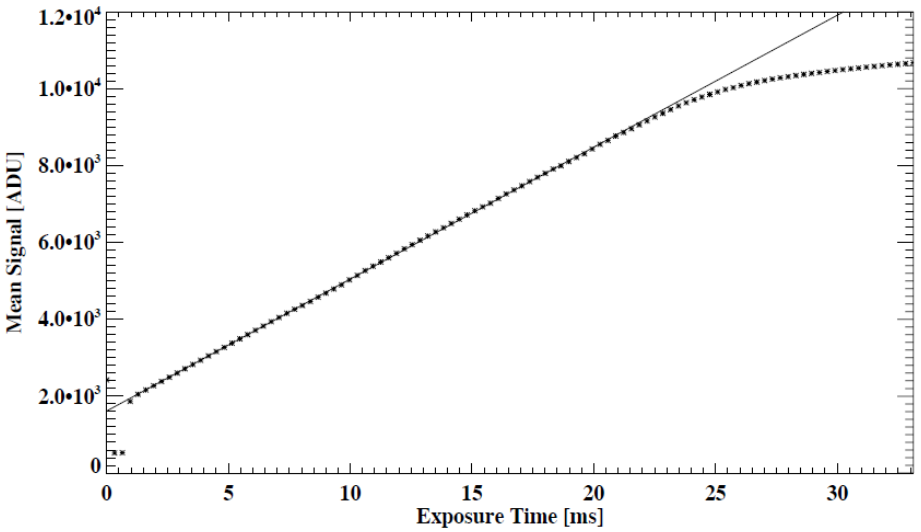
2.5 Defects

- *Dark/bright columns are caused by traps of electrons during image readout.*
- *Stuck pixel: a pixel that always reads high on all exposures.*
- *Hot pixel: a pixel that reads high on longer exposures.*
- *Dead pixel: a pixel that reads zero (black) on all exposures.*
- *Defects can't be corrected by flat fielding.*
- *Defects can be removed by calibration.*



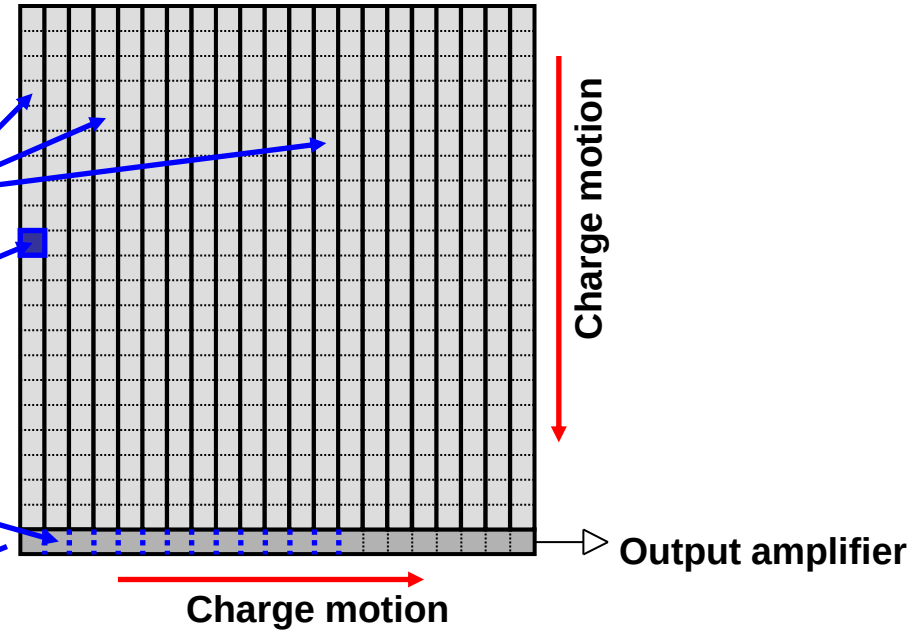
2.6 Linearity

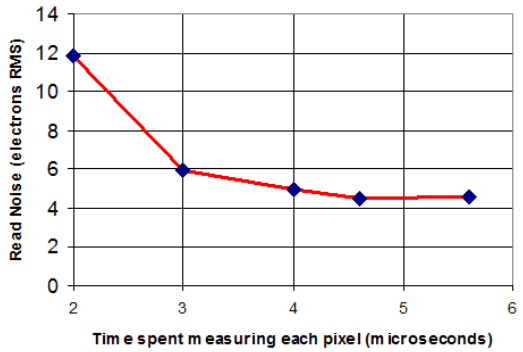
- *Linearity is a measure of how consistently the CCD/CMOS responds to light over its well depth.*
  - *Low light level: readout noise*
  - *Linear range*
  - *High light level: non-linear flattening when the charge in the well > 80%*
  - *Extremely high light level: saturation*
- *If uncertain of the linear range of a CCD/CMOS, it is best to measure it*
- *Method of obtaining a linearity curve:*
  - *Use stable light source or stars*
  - *Obtain consecutively increasing exposures*
  - *Plot output ADU vs. exposure time*



$$nonlinearity(\%) = \frac{Max(+)Deviation + Max(-)Deviation}{MaximumSignal}$$

2.7 Readout Noise





- *Readout noise is mainly due to Johnson noise in on-chip amplifier and A/D circuit.*
- *Readout noise: in terms of the number of electrons.*
- *This noise can be reduced by reducing the bandwidth, but this requires that readout is slower.*
- *Readout noise is added into every pixel every time the array is read out.*
- *Signal-to-noise ratio*

$$SNR = \frac{n_{pe}}{\sqrt{n_{pe} + N_{RN}^2 + N_{Dark}^2 + (Un_{pe})^2}}$$

Dynamic Range

- *Dynamic Range defined as the ratio between the brightest and faintest detectable signal.*

$$DR = \frac{V_{\max}}{V_{noise}} = \frac{N_{fullwell}}{N_{RN}}$$

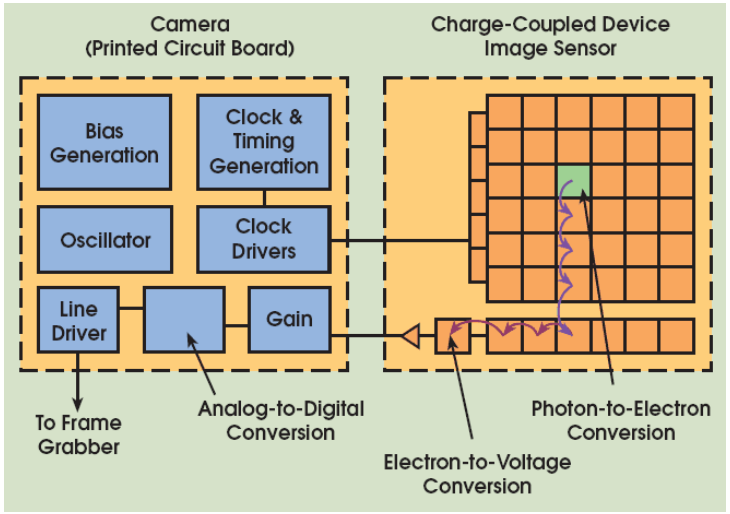
- *Dynamic range is simplified as the ratio of full well and readout noise*
- *Dynamic range has no unit, but often expressed in decibels,*

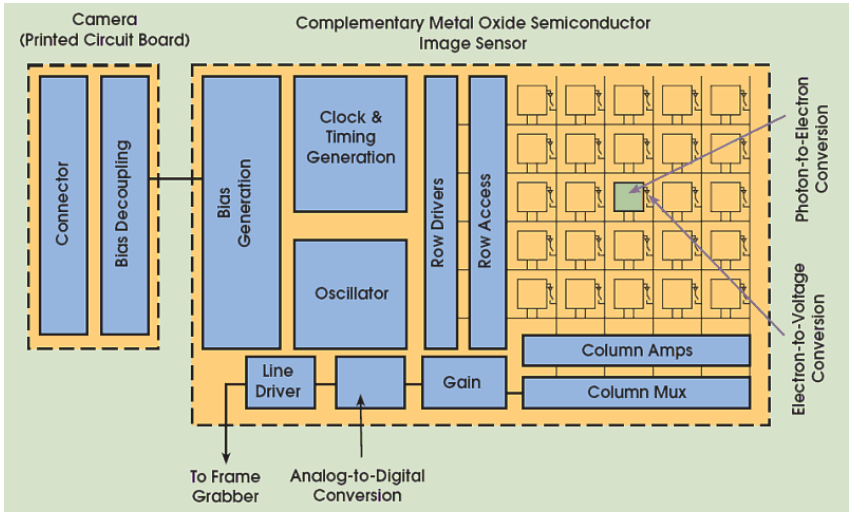
$$DR = 20\log\left(\frac{N_{fullwell}}{N_{RN}}\right) dB$$

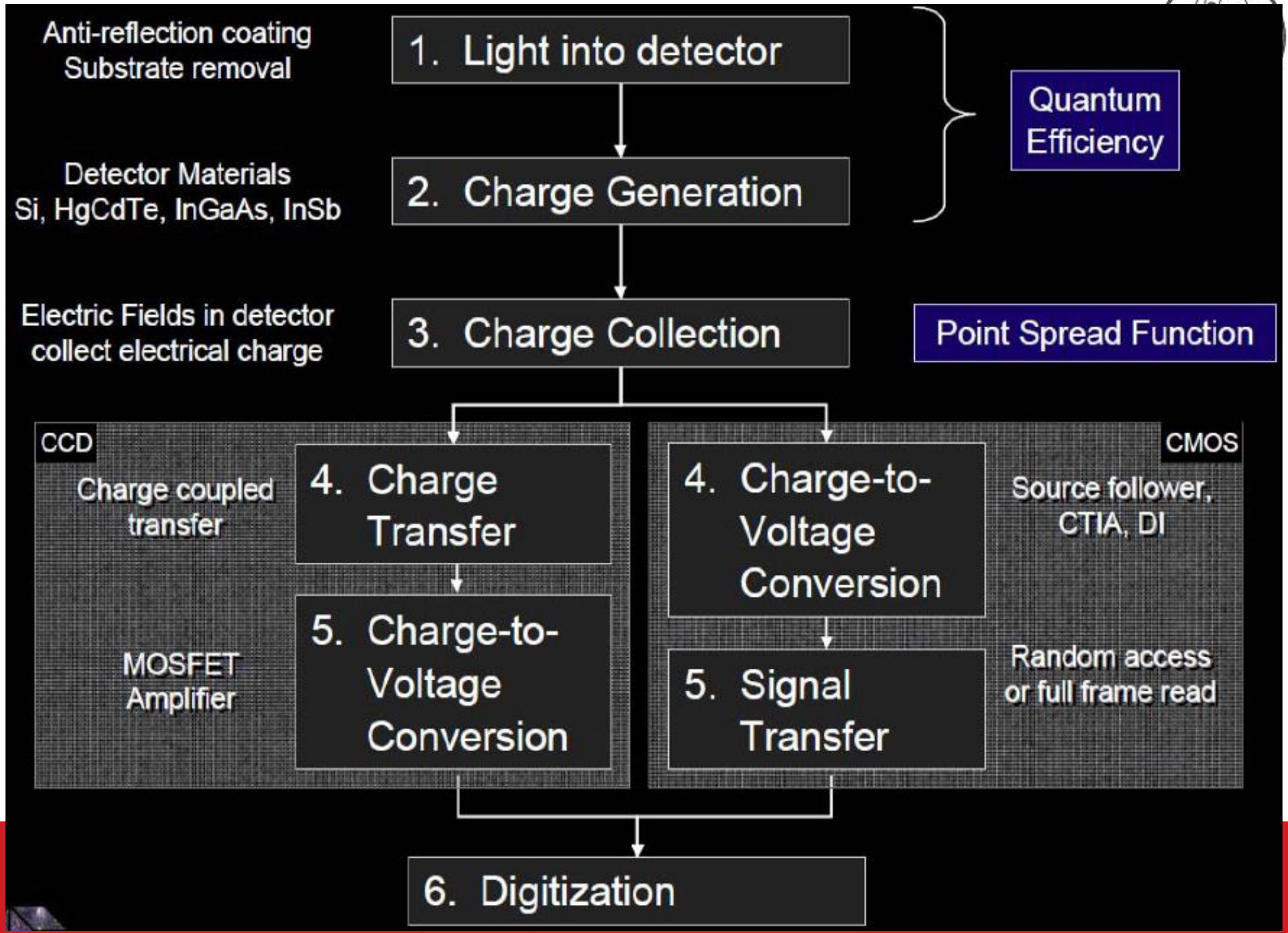
- *A CCD array has a full well of 150,000 e-. The advertised dynamic range is 80dB. Could you estimate its readout noise?*

3.1 CMOS vs CCD

- *CMOS: Complementary Metal Oxide Semiconductor*
- *CCD: Charge Coupling Device*
- *Both are pixelated MOS and have the same process in charge generation and charge collection*
- *However, charge transfer and charge detection are different*
- *CCD: all pixels share one charge-to-voltage converter*
- *CMOS: every pixel has its own charge-to-voltage converter*






Anti-reflection coating
Substrate removal
1. Light into detector
Detector Materials
Si, HgCdTe, InGaAs, InSb
2. Charge Generation
Quantum Efficiency
Electric Fields in detector collect electrical charge
3. Charge Collection
Point Spread Function
CCD
Charge coupled transfer
4. Charge Transfer
MOSFET Amplifier
5. Charge-to-Voltage Conversion
CMOS
4. Charge-to-Voltage Conversion
Source follower, CTIA, DI
5. Signal Transfer
Random access or full frame read
6. Digitization

Pros and Cons

CCD

- *offer high-quality, low-noise images*
- *greater sensitivity and fidelity*
- *100 times more power*
- *acceptable speed*
- *complicated anti-blooming technique*
- *require specialized assembly lines*
- *equal reliability*
- *older and more developed technology*

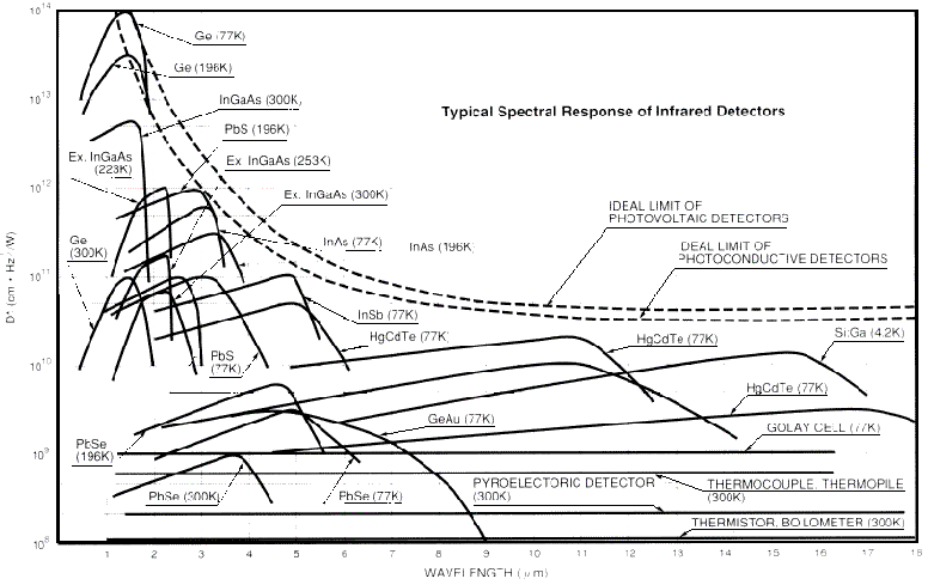
CMOS

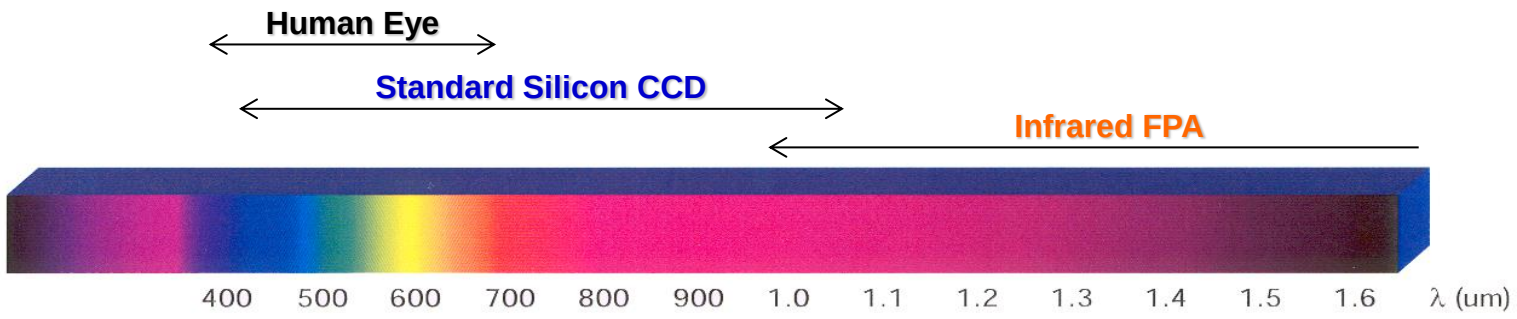
- *more susceptible to noise*
- *light sensitivity is lower*
- *consume little power*
- *much fast*
- *natural blooming immunity*
- *easy to manufacture*
- *highly integrated*
- *less expensive*

- *CMOS imagers offer superior integration, power dissipation and system size at the expense of image quality (particularly in low light) and flexibility. They are the technology of choice for high-volume, space-constrained applications where image quality requirements are low.*
- *CCDs offer superior image quality and flexibility at the expense of system size. They remain the most suitable technology for high-end imaging applications.*

3.2 IRFPA

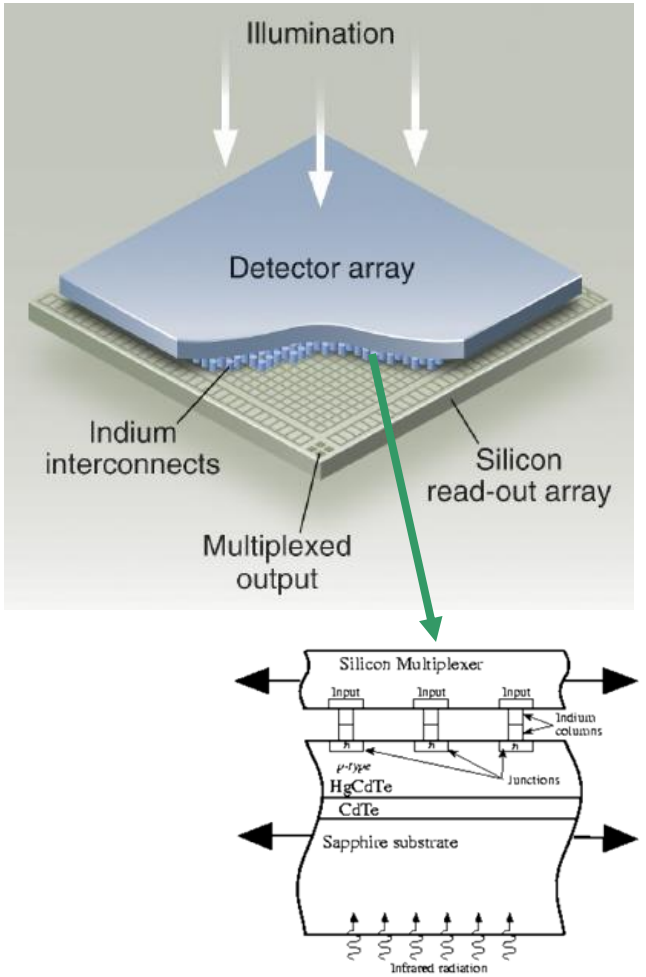
- *IRFPA: InfraRed Focal Plane Array*
- *Silicon CCD/CMOS detectors are unable to sensor photons in the infrared*
- *Which material for NIR ?*
  - *HgCdTe*
  - *InSb*
  - *PtSi*
  - *InGaAs*
  - *……*





Hybrid IRFPA

- *IRFPAs mostly deploy hybrid structure*
  - *Photosensitive substrate*
  - *Silicon read-out circuit*
- *Sapphire Substrate*
  - *Array of n-p-photodiodes made from HgCdTe (epitaxially grown on transparent carrier (AlsO3/CdTe, CdZnTe/CdTe))*
  - *Boron implants to define pixel structure*
  - *Read-out Circuit (ROIC)*
  - *Si based integrated circuit (CMOS array) with individually addressable pixels*
- *Flip-chip Technique*
  - *Substrate and ROIC are electrically connected pixel by pixel*
  - *Indium bumps*



4. Observation with Solid State Detectors

$$image(x,y) = \frac{raw(x,y) - dark(x,y)}{flat(x,y)}$$

- *CCD, CMOS, IRFPA Imaging*
- *Dark Fielding*
- *Flat Fielding*
- *Image Reduction*